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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,387	02/02/2001	Stanley N. Protigal	2898.2US (88-070.7)	2208

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/776,387	Applicant(s) PROTIGAL ET AL.	
	Examiner A. Sefer	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5 and 8-10* is/are allowed.

6)☒ Claim(s) *1,2,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. US Patent No. 4,737,830.

Patel et al disclose (figs. 3-12 and claim 1) a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate 28; and a semiconductor device secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor 16 including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Hoashi (JP 61-269317)

Hoashi discloses in figs. 1-8 a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate; and a semiconductor device 12 secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor C including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

4. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. US Patent No. 4,737,830.

Patel et al disclose (figs. 3-12 and claim 1) semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate 28; active circuit devices on the semiconductor substrate; and a capacitor 16 having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate.

5. Claim 6 is rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. US Patent No. 4,737,830.

Patel et al disclose (figs. 3-12 and claim 1) a semiconductor die assembly for connection to external circuitry, the semiconductor die assembly comprising a carrier substrate configured for providing power Vcc and ground Vss for at least one semiconductor die operably connected

thereto; and at least one semiconductor die connected to the carrier substrate and including a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 16 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance the at least one semiconductor die.

6. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Patel et al. US Patent No. 4,737,830.

Patel et al disclose (figs. 3-12 and claim 1) a semiconductor device for connection to a carrier substrate configured power Vcc and Vss thereto, the semiconductor device comprising a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 16 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefore when the semiconductor device is operably connected to a carrier substrate.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. US Patent No. 4,903,113 in view of RD 254042.

Frankeny et al disclose in figs. 1-7 a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate 64; and a semiconductor device 70 secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an a chip capacitor 58, the chip capacitor being operably coupled between the active devices and the carrier substrate, but do not disclose an on-chip capacitor.

RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ on-chip capacitors since that would minimize series inductance and provide an effective noise filtering means via bypass capacitor.

9. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clayton US Patent No. 4,656,605 in view of RD 254042.

Clayton discloses (see figs. 1 and 2 and col. 2, lines 42-48) a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate; and a semiconductor device 10 secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and a chip capacitor 33, the chip capacitor being operably coupled between the active devices, but do not disclose an on-chip capacitor.

RD 254042 teaches the benefit of on-chip capacitors as an alternative to off-chip capacitor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to employ on-chip capacitors since that would minimize series inductance and provide an effective noise filtering means via bypass capacitor.

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clayton US Patent No. 4,656,605 in view of RD 254042.

Clayton discloses (see figs. 1 and 2 and col. 2, lines 42-48) a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate; active circuit devices 10-18 on the semiconductor substrate; and a capacitor 33, the capacitor being operably coupled to the active circuit devices, but does not specifically disclose a capacitor being formed in an active area of a semiconductor substrate.

RD 254042 teaches the benefit of forming a capacitor in an active area of a semiconductor substrate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to form a capacitor in an active area of a semiconductor substrate.
since that would minimize series inductance and provide an effective noise filtering means via bypass capacitors.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. US Patent No. 4,903,113 in view of RD 254042.

Frankeny et al disclose in figs. 1-7 a semiconductor die assembly for connection to external circuitry, the semiconductor die assembly comprising a carrier substrate configured for providing power 60 and ground 62 for at least one semiconductor die 70

operably connected thereto; and at least one semiconductor die connected to the carrier substrate and including a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 58 on the semiconductor substrate, at least one capacitor operably connected to the active circuit elements, but do not specifically disclose a capacitor being formed in an active area of semiconductor substrate.

RD 254042 teaches the benefit of forming a capacitor in an active area of a semiconductor substrate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to form a capacitor in an active area of a semiconductor substrate.
since that would minimize series inductance and provide an effective noise filtering means via bypass capacitors.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. US Patent No. 4,903,113 in view of RD 254042.

Frankeny et al disclose in figs. 1-7 a semiconductor device for connection to a carrier substrate configured power 60 and ground 62 thereto, the semiconductor device comprising a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 58 on the semiconductor substrate, at least one capacitor operably connected to the active circuit elements, but do not specifically disclose a capacitor being formed in an active area of semiconductor substrate.

RD 254042 teaches the benefit of forming a capacitor in an active area of a semiconductor substrate.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to form a capacitor in an active area of a semiconductor substrate.
since that would minimize series inductance and provide an effective noise filtering means via bypass capacitors.

Allowable Subject Matter

13. Claims 3-6 and 8-10 are allowed.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Muggli et al. USPN 4,720,467 disclose an IC device with on-chip capacitor.

b. Heeren USPN 3,893,146 disclose a Memory device including on-chip capacitors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
July 16, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800